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04609945 E.I. No: EIP97013500029

Title: Monolithic 16-bit A/D converter

Author: Ruoxu, Wang

Corporate Source: Sichuan Inst of Solid-State Circuits, China

Conference Title: Proceedings of the 1996 2nd International Conference on ASIC

Conference Location: Shanghai, China Conference Date: 19961021-19961024

Sponsor: IEEE

E.I. Conference No.: 45949

Source: International Conference on ASIC, Proceedings 1996. Shanghai Scientific and Technological Literature Publishing House, Shanghai, China. p 256-259

Publication Year: 1996

CODEN: 002513

Language: English

Document Type: CA; (Conference Article) Treatment: X; (Experimental)

Journal Announcement: 9703W3

Abstract: A 16-bit successive-approximation-type monolithic A/D converter is described. In the internal D/A converter a dynamic current divider based on dynamic element matching is used to obtain the required high accuracy of the six **most significant** bits. To construct the ten **least significant** bits a master-slave ladder and passive **divider** network based on emitter scaling of transistors is used. The successive approximation register (SAR) is capable of achieving high-speed conversion without the use of clock-controlled logic circuits. The conversion time is about 15 μ s. Both the linearity and differential linearity errors are less than 0.0015%FSR. The chip is processed in a standard p-n junction isolated 3 μ m bipolar technology and the die size is 5.12 multiplied by 6.12 mm**2. (Author abstract) 6 Refs.

Descriptors: *Electric converters; Monolithic integrated circuits; Analog to digital conversion; Dividing circuits (arithmetic); Ladder networks; Passive networks; Integrated circuit layout; Semiconductor junctions

Identifiers: Monolithic analog to digital converters; Current divider; Successive approximation register; Conversion time; Differential linearity errors

Classification Codes:

714.2 (Semiconductor Devices & Integrated Circuits); 721.3 (Computer Circuits); 703.1 (Electric Networks)

714 (Electronic Components); 721 (Computer Circuits & Logic Elements); 703 (Electric Circuits)

71 (ELECTRONICS & COMMUNICATIONS); 72 (COMPUTERS & DATA PROCESSING); 70 (ELECTRICAL ENGINEERING)

10/5/2 (Item 2 from file: 8)
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04513078 E.I. No: EIP95052693425

Title: Full-frame compression of discrete wavelet and cosine transforms

Author: Lo, Shih-Chung B.; Li, Huai; Krasner, Brian H.; Freedman, Matthew T.; Mun, Seong K.

Corporate Source: Georgetown Univ. Medical Cent., Washington, DC, USA

Conference Title: Medical Imaging 1995: Image Display

Conference Location: San Diego, CA, USA Conference Date: 19950226-19950228

Sponsor: SPIE - Int Soc for Opt Engineering, Bellingham, WA USA

E.I. Conference No.: 22242

Source: Proceedings of SPIE - The International Society for Optical Engineering v 2431 1995. Society of Photo-Optical Instrumentation Engineers, Bellingham, WA, USA. p 195-202

Publication Year: 1995

CODEN: PSISDG ISSN: 0277-786X ISBN: 0-8194-1779-3

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 9611W4

Abstract: At the foreground of computerized radiology and the filmless hospital are the possibilities for easy image retrieval, efficient storage, and rapid image communication. This paper represents the authors' continuous efforts in compression research on full-frame discrete wavelet (FFDWT) and full-frame discrete cosine transforms (FFDCT) for medical image compression. Prior to the coding, it is important to evaluate the global entropy in the decomposed space. It is because of the minimum entropy, that a maximum compression efficiency can be achieved. In this study, each image was split into the top three most significant bit (MSB) and the remaining remapped least significant bit (RLSB) images. The 3MSB image was compressed by an error-free contour coding and received an average of .1 bit/pixel. The RLSB image was either transformed to a multi-channel wavelet or the cosine transform domain for entropy evaluation. Ten x-ray chest radiographs and ten mammograms were randomly selected from our clinical database and were used for the study. Our results indicated that the coding scheme in the FFDCT domain performed better than in FFDWT domain for high-resolution digital chest radiographs and mammograms. From this study, we found that decomposition efficiency in the DCT domain for relatively smooth images is higher than that in the DWT. However, both schemes worked just as well for low resolution digital images. We also found that the image characteristics of the 'Lena' image commonly used in the compression literature are very different from those of radiological images. The compression outcome of the radiological images can not be extrapolated from the compression result based on the 'Lena'. 18 Refs.

Descriptors: Medical imaging; Image compression; Mathematical transformations; Radiology

Identifiers: Cosine transform; Computerized radiography; Mammograms; Radiographs; Coding scheme

Classification Codes:

461.1 (Biomedical Engineering); 723.2 (Data Processing); 741.3 (Optical Devices & Systems); 622.3 (Radioactive Material Applications); 461.6 (Medicine)

461 (Biotechnology); 723 (Computer Software); 741 (Optics & Optical Devices); 622 (Radioactive Materials)

46 (BIOENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 74 (OPTICAL TECHNOLOGY); 62 (NUCLEAR TECHNOLOGY)

10/5/3 (Item 3 from file: 8)

DIALOG(R) File 8: Ei Compendex(R)

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04333733 E.I. No: EIP96013008444

Title: Contour coding and full-frame compression of discrete wavelet and cosine transforms

Author: Lo, Shih-Chung B.; Li, Huai; Krasner, Brian H.; Freedman, Matthew T.; Mun, Seong K.

Corporate Source: Georgetown Univ Medical Cent, Washington, DC, USA

Conference Title: Proceedings of the 1995 IEEE International Conference on Image Processing. Part 2 (of 3)

Conference Location: Washington, DC, USA Conference Date:

1995-10-10/10/96

Publisher: IEEE

Conf. Conference No.: 44184

Source: IEEE International Conference on Image Processing v 2 1996. IEEE, Los Alamitos, CA, USA, 95CB35819. p 9-12

Publication Year: 1996

CODEN: 85QTAW

Language: English

Document Type: CA; (Conference Article) Treatment: T; (Theoretical)

Journal Announcement: 9603W3

Abstract: This paper represents the authors' research on a hybrid method combined with contour coding, full-frame discrete wavelet (FFDWT) and full-frame discrete cosine transforms (FFDCT) for medical image compression. In this study, ten x-ray chest radiographs and ten mammograms

were randomly selected from our clinical database. Each image was **split** into the top three **most significant** bit (MSB) and the remaining was remapped to **least significant** bit (RLSB) image. The 3MSB image was compressed by an error-free contour coding and received an average of 0.1 bit/pixel. The RLSB image was either transformed to a multi-channel wavelet or the cosine transform domain for entropy evaluation and compression.

(Author abstract) 12 Refs.

Descriptors: *Medical imaging; Image coding; Image compression; Wavelet transforms; Medical computing; Coding errors; Database systems; Algorithms; Error analysis; Radiography

Identifiers: Contour coding; Full frame compression; Discrete wavelet; Cosine transforms; Mammograms; Most significant bit; Least significant bit; Mean square error

Classification Codes:

461.1 (Biomedical Engineering); 723.2 (Data Processing); 921.3 (Mathematical Transformations); 723.3 (Database Systems); 921.6 (Numerical Methods)

461 (Biotechnology); 723 (Computer Software); 921 (Applied Mathematics)

46 (BIOENGINEERING); 72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

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DIAGN(R)File 8:EI Compendex(R)

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04219972 E.I. No: EIP95082806227

Title: **Position detection with the use of MAGFET's**

Author: Kaulberg, Thomas; Bogason, Gudmundur

Corporate Source: Technical Univ of Denmark, Lyngby, Den

Conference Title: Proceedings of the 1995 IEEE Instrumentation and Measurement Technology Conference

Conference Location: Naltham, MA, USA Conference Date: 19950423-19950426

Sponsor: IEEE

E.I. Conference No.: 43336

Source: Conference Record - IEEE Instrumentation and Measurement Technology Conference 1995. IEEE, Piscataway, NJ, USA, 95CH35783. p 158-162

Publication Year: 1995

CODEN: CRIIE7

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T; (Theoretical)

Journal Announcement: 9509W5

Abstract: An angledetector with a digital output is described. The component is meant as an alternative to the traditional slide potentiometer used as volume control in many hearing aid applications. The component is based on the use of magnetic field sensitive MOSFET's (MAGFET's) detecting the position of a tiny bar magnet placed above a silicon chip. Because of the galvanic separation between the angle-setting bar magnet and the electrical circuit, this component is insensitive to the rather hostile environment hearing aids are exposed to. The lifetime of the component is thereby increased significantly. The electrical circuit contains a switched current A/D - D/A conversion system for offset compensating the MAGFET's and for converting the MAGFET signal currents into a digital output proportional to the input angle. It is implemented using a commercially available 1.5 mu m CMOS process. (Author abstract) 5 Refs.

Descriptors: *Sensors; MOSFET devices; Magnetic devices; Hearing aids; Magnetic fields; Analog to digital conversion; Digital to analog conversion; Computer simulation; Transfer functions; Finite element method

Identifiers: Position detection; MAGFETs; Bar magnet; **Most significant** bit; Angle detector; Magnetic flux; **Least significant** bit; Galvanic contact; Galvanic **separation**

Classification Codes:

732.2 (Control Instrumentation); 714.2 (Semiconductor Devices & Integrated Circuits); 708.4 (Magnetic Materials); 701.2 (Magnetism: Basic Concepts & Phenomena); 723.2 (Data Processing); 723.5 (Computer

Applications)

732 (Control Devices); 714 (Electronic Components); 708 (Electric & Magnetic Materials); 701 (Electricity & Magnetism); 723 (Computer Software)

73 (CONTROL ENGINEERING); 71 (ELECTRONICS & COMMUNICATIONS); 70 (ELECTRICAL ENGINEERING); 72 (COMPUTERS & DATA PROCESSING)

10/5/5 (Item 5 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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03919810 E.I. No: EIP94081364885

Title: **Parallel simulation of heterogeneous arithmetic units networks and high precision dot products**

Author: Fiallos Aguilar, M.; Duprat, J.

Corporate Source: LIP, Lyon, Fr

Conference Title: Proceedings of the IEEE 27th Annual Simulation Symposium

Conference Location: La Jolla, CA, USA Conference Date: 19940411-19940415

Sponsor: Society for Computer Simulation (SCS); IEEE Computer Society; Association for Computing Machinery (ACM)

E.I. Conference No.: 20768

Source: Proceedings of the IEEE Annual Simulation Symposium 1994. Publ by IEEE, Computer Society Press, Los Alamitos, CA, USA, 94TH0642-9. p 13-22

Publication Year: 1994

CODEN: 001580 ISSN: 0272-4715 ISBN: 0-8186-5620-4

Language: English

Document Type: CA; (Conference Article) Treatment: A; (Applications); T; (Theoretical)

Original Announcement: 9409W5

Abstract: In this paper we deal with a new high precision computation of the dot product. The key idea is to use hundreds of digit-serial arithmetic units or operators that allow a 'massive' digit-level pipelining. Parallel discrete-event simulations performed on a memory-distributed massively parallel computer show that with a limited number of arithmetic units, the computation of dot product when performed using a 'classical' algorithmic technique (i.e. serial cumulative multiplications) is almost as fast as the case where an 'optimal' divide-and-conquer algorithmic technique is used. Interconnection networks for both algorithmic techniques are considered. (Author abstract) 16 Refs.

Descriptors: *Computer simulation; Digital arithmetic; Pipeline processing systems; Parallel processing systems; Algorithms; Digital storage; Adders; Multiplying circuits; Computational methods; Online systems

Identifiers: Parallel simulation; Heterogeneous arithmetic units networks; High precision dot products; Digit level pipelining; Memory distributed massively parallel computer; **Divide** and conquer algorithmic technique; Digit on line; **Most significant** digit; **Least significant** digit

Classification Codes:

723.5 (Computer Applications); 921.6 (Numerical Methods); 722.4 (Digital Computers & Systems); 722.1 (Data Storage, Equipment & Techniques); 721.3 (Computer Circuits); 721.1 (Computer Theory, Includes Formal Logic, Automata Theory, Switching Theory, Programming Theory)

723 (Computer Software); 921 (Applied Mathematics); 722 (Computer Systems); 721 (Computer Circuits & Logic Elements)

72 (COMPUTERS & DATA PROCESSING); 92 (ENGINEERING MATHEMATICS)

10/5/6 (Item 6 from file: 8)

DIALOG(R)File 8:EI Compendex(R)

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02769115 E.I. Monthly No: EI8908079381

Title: **Video communication terminal for a high-speed X.25 packet switching system.**

Author: Kishino, Fumio; Kanemaki, Naobumi; Hotta, Eiichi

Corporate Source: NTT Human Interface Lab, Jpn
Source: Denki Tsushin Kenkyusho Kenkyu Jitsuyoka Hokoku/Electrical
Communications Laboratories Review v 38 n 3 1989 p 239-248
Publication Year: 1989
CODEN: DTKKAA ISSN: 0415-3200
Language: Japanese
Document Type: JA; (Journal Article) Treatment: A; (Applications)
Journal Announcement: 8908

Abstract: This paper describes a video communication terminal for an experimental high-speed multi-media packet switching system based on the X.25 protocol. Video signals are variable bit-rate coded and transmitted in the packet format. Picture quality is improved by transmitting video signals as they are generated. Two-channel audio signals in the 7 kHz band are digitized and transmitted in a packet format. Packet losses are compensated for by the demand refresh method for video signals, and by separating into most significant parts and least significant parts for audio signals. (Author abstract) 6 Refs. In Japanese.

Descriptors: *SIGNAL RECEIVERS--*Design; DIGITAL COMMUNICATION SYSTEMS; DATA TRANSMISSION--Packet Switching

Identifiers: HIGH SPEED PACKET SWITCHING; VIDEO COMMUNICATION TERMINAL; X.25 PROTOCOL; VIDEO SIGNALS; AUDIO SIGNALS

Classification Codes:

741 (Telephone & Line Communications); 741 (Optics & Optical Devices);
741 (Sound Equipment & Systems)
741 (ELECTRONICS & COMMUNICATIONS); 74 (OPTICAL TECHNOLOGY); 75
(ACOUSTICAL TECHNOLOGY)

10/5/7 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
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5565704 INSPEC Abstract Number: B9706-1265H-005, C9706-5180-003

Title: **A monolithic 16-bit A/D converter**

Author(s): Wang Ruoxu

Author Affiliation: Sichuan Inst. of Solid-State Circuits, Chongqing, China

Conference Title: 1996 2nd International Conference on ASIC Proceedings (IEEE Cat. No.96TH8140) p.256-9

Editor(s): Zhang Qian-Ling; Tang Ting-Ao; Yu Huihua

Publisher: Shanghai Sci. & Technol. Literature Publishing House, Shanghai, China

Publication Date: 1996 Country of Publication: China 452 pp.

Material Identity Number: XX96-03455

Conference Title: Proceedings of 2nd International Conference on ASIC

Conference Sponsor: Chinese Inst. Electron.; IEEE Beijing Sect.; Nat. Natural Sci. Found. China; K.C. Wong Educ. Found., Hong Kong; IEE Electron. Div.; IEEE Circuits & Syst. Soc.; ACM SIGDA

Conference Date: 21-24 Oct. 1996 Conference Location: Shanghai, China

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P)

Abstract: a 16-bit successive-approximation-type monolithic A/D converter is described. In the internal D/A converter a dynamic current divider based on dynamic element matching is used to obtain the required high accuracy of the six most significant bits. To construct the ten least significant bits a master-slave ladder and passive divider network based on emitter scaling of transistors is used. The successive approximation register (SAR) is capable of achieving high-speed conversion without the use of clock-controlled logic circuits. The conversion time is about 15 μ s. Both the linearity and differential linearity errors are less than 0.0015% FSR. The chip is processed in a standard p-n junction isolated 3 μ m bipolar technology and the die size is 5.12*6.12 mm/sup 2/. (6 Refs)

Subfile: B C

Descriptors: analogue-digital conversion; bipolar integrated circuits; isolation technology

Identifiers: monolithic A/D converter; successive-approximation-type; dynamic current divide; dynamic element matching; master-slave ladder;

passive divider network; high-speed conversion; p-n junction isolated bipolar technology; bipolar ADC; 16 bit; 3 micron; 15 mus

Class Codes: B1265H (A/D and D/A convertors); B2570B (Bipolar integrated circuits); C5180 (A/D and D/A convertors)

Numerical Indexing: word length 1.6E+01 bit; size 3.0E-06 m; time 1.5E-05 s

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DIALOG(R)File 2:INSPEC

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4487600 INSPEC Abstract Number: B9311-6140C-036

Title: CCITT H.261 compatible mixed bit rate coding of video for ATM networks

Author(s): Minami, S.

Author Affiliation: Toshiba Corp., Kawasaki, Japan

Conference Title: SUPERCOMM/ICC '92. Discovering a New World of Communications (Cat. No.92CH3132-8) p.537-43 vol.1

Publisher: IEEE, New York, NY, USA

Publication Date: 1992 Country of Publication: USA 4 vol. (xxxv+xxxv+xxxv+xviii+1913) pp.

ISBN: 0 7803 0599 X

U.S. Copyright Clearance Center Code: CH3132-8/0000-0537\$03.00

Conference Sponsor: IEEE

Conference Date: 14-18 June 1992 Conference Location: Chicago, IL, USA

Language: English Document Type: Conference Paper (PA)

Treatment: Practical (P); Theoretical (T); Experimental (X)

Abstract: A mixed bit rate (MBR) video coding method is presented for asynchronous transfer mode (ATM) networks which has communication compatibility between constant bit rate (CBR) video codecs and variable bit rate (VBR) codecs. In MBR video coding, essential information is encoded at a CBR by using a conventional CBR coding method such as H.261 and enhancement information is encoded at a VBR to attain constant image quality. To realize the MBR coding of video, the conventional embedded pulse code modulation (PCM) quantization is extended by applying the requantization method only to the least significant bit (LSB) of the quantizer output. In the EX-EMB PCM method, the most significant part and least significant part (MSP/LSP) separation of embedded PCM and an additional threshold for the requantizer are dynamically determined to attain a desired distortion. The MBR codec with EX-EMB PCM was evaluated by computer simulations. The simulation results showed that the proposed method was effective not only for improving video quality but also it prevented the degradations of image quality at the scene change by increasing the bit rate for the VBR channel. (13 Refs)

Profile: B

Descriptors: asynchronous transfer mode; codecs; image coding; telecommunication networks; video signals

Identifiers: mixed bit rate video coding; PCM quantization; ATM networks; CCITT H.261; MBR; asynchronous transfer mode; communication compatibility; constant bit rate; CBR; video codecs; variable bit rate; VBR; image quality; pulse code modulation; requantization method; least significant bit; LSB; computer simulations; video quality

Class Codes: B6140C (Optical information and image processing); B6120B (Codes); B6220 (Stations and subscriber equipment); B6430 (Television equipment, systems and applications); B6210 (Telecommunication applications)

10/5/9 (Item 3 from file: 2)

DIALOG(R)File 2:INSPEC

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04390023 INSPEC Abstract Number: B9306-6430-001

Title: A variable bit rate video codec for ATM networks and its robustness against cell losses

Author(s): Manabe, K.; Tanaka, T.; Ohtsuka, S.

Author Affiliation: NTT Human Interface Labs., Yokosuka, Japan
Journal: Transactions of the Institute of Electronics, Information and
Communication Engineers B-I vol.J76B-I, no.1 p.40-7
Publication Date: Jan. 1993 Country of Publication: Japan
CODEN: DJBTES
Language: Japanese Document Type: Journal Paper (JP)
Treatment: Practical (P); Experimental (X)
Abstract: A variable bit rate video codec is developed for ATM
(asynchronous transfer mode) networks. Several techniques are adopted
against the cell losses that in traditional codecs catastrophically damage
reproduced image quality. The cell loss robustness is tested by subjective
picture quality assessment for several conditions. An information
packetization technique with cyclic memory refresh provides MOS 3.5 picture
quality for cell loss ratio values lower than 10^{-6} . A layered coding
technique, in which DCT (discrete cosine transform) coefficients are
divided into MSP (most significant parts) and LSP (least
significant parts), provides additional cell loss robustness. This
ensures robustness for cell loss ratio values lower than 10^{-4} . (15
Refs)
Subfile: B
Descriptors: asynchronous transfer mode; codecs; discrete cosine
transforms; image coding; video equipment
Identifiers: DCT coefficients; ATM networks; variable bit rate video;
asynchronous transfer mode; reproduced image quality; cell loss robustness;
subjective picture quality assessment; information packetization; cyclic
memory refresh; MOS 3.5 picture quality; cell loss ratio; layered coding
technique; discrete cosine transform; most significant parts; least
significant parts
Class Codes: B6430 (Television equipment, systems and applications);
B6220 (Stations and subscriber equipment); B0290Z (Other numerical methods
)

10/5/10 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC
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03408051 INSPEC Abstract Number: B89050080

Title: **Variable-bit-rate coding capable of compensating for packet loss**
Author(s): Shimamura, K.; Hayashi, Y.; Kishino, F.
Author Affiliation: NTT Human Interface Labs., Kanagawa, Japan
Journal: Proceedings of the SPIE - The International Society for Optical
Engineering vol.1001, pt.2 p.991-8
Publication Date: 1988 Country of Publication: USA
CODEN: PSISDG ISSN: 0277-786X
Conference Title: Visual Communications and Image Processing '88
Conference Sponsor: SPIE
Conference Date: 9-11 Nov. 1988 Conference Location: Cambridge, MA,
USA

Language: English Document Type: Conference Paper (PA); Journal Paper
(JP)

Treatment: Theoretical (T); Experimental (X)
Abstract: Asynchronous transfer mode (ATM) is expected to be one of the
important variable-bit-rate methods for video transmission. Packet loss has
the greatest influence on picture quality in a video network. The authors
propose a layered coding technique suitable for ATM using discrete cosine
transform (DCT) coding. The proposed layered coding separates coded
information into most significant parts (MSPs) and least significant
parts (LSPs) and gives MSP packets priority over LSP packets to reduce the
influence of packet loss on picture quality. The influence of packet loss
on picture quality is also described, and the effectiveness of the proposed
layered coding is confirmed with decoded pictures. (2 Refs)

Subfile: B
Descriptors: encoding; ISDN; packet switching; picture processing; video
signals
Identifiers: B-ISDN; asynchronous transfer code; packet loss; video
transmission; picture quality; video network; layered coding technique;
discrete cosine transform

Class Codes: B6140C (Optical information processing); B6120B (Codes);
B6150 (Communication switching theory); B6210M (ISDN)

10/5/11 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC
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02578214 INSPEC Abstract Number: B86001182, C86003139

Title: A high performance bipolar multiplier

Author(s): Bielawski, J.; Wang, T.

Author Affiliation: Nat. Semicond., Santa Clara, CA, USA

Conference Title: Southcon/85 and Mini/Micro Southeast Conference Record
p.12/1/1-4

Publisher: Electron. Conventions Manage, Los Angeles, CA, USA

Publication Date: 1985 Country of Publication: USA 898 pp.

Conference Sponsor: IEEE; ERA

Conference Date: 5-7 March 1985 Conference Location: Atlanta, GA, USA

Language: English Document Type: Conference Paper (PA)

Relevance: Practical (P)

Abstract: A high performance 16*16 bipolar TTL multiplier has been designed by the National Semiconductor Corporation. This NSC 16*16 TTL parallel multiplier is capable of a 30 ns cycle time in pipeline operation. It can accommodate operands of two's complement, unsigned magnitude, or mixed mode. Both the input and output registers have separate clocks. A feed through control is included to provide transparent output registers. The full 32-bit product is split into a 16-bit least significant product (LSP) and a 16-bit most significant product (MSP) which can be rounded. The MSP and LSP can be multiplexed to the output port. The LSP output port is common I/O with the multiplier inner port. A register shift control provides 32-bit two's complement capability. (3 Refs)

Subfile: B C

Descriptors: bipolar integrated circuits; digital integrated circuits; integrated logic circuits; pipeline processing; transistor-transistor logic
Identifiers: digital IC; bipolar multiplier; TTL; National Semiconductor Corporation; 30 ns cycle time; pipeline operation; feed through control; transparent output registers; full 32-bit product; 16-bit least significant product; 16-bit most significant product; register shift control; two's complement capability

Class Codes: B1265B (Logic circuits); B1265Z (Other digital circuits);
B2570B (Bipolar integrated circuits); C5120 (Logic and switching circuits)
; C5230 (Digital arithmetic methods)

10/5/12 (Item 1 from file: 94)
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01720536 JICST ACCESSION NUMBER: 93A0215616 FILE SEGMENT: JICST-E
Installing Leaky prediction to the motion picture coding method NUCLEI for ATM networks.

FUJIMURA MAKOTO (1); SHIMODA YUTAKA (1); KURODA HIDEO (1); MWANSA D (1)
(1) Nagasaki Univ., Faculty of Engineering

Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report
(Institute of Electronics, Information and Communication Engineers),
1993, VOL.92,NO.438(IE92 105-114), PAGE.63-69, FIG.5, TBL.1, REF.13

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ABSTRACT: Recently, motion picture coding methods for an ATM(Asynchronous Transfer Mode) networks of a broad band ISDN are studied actively. This paper describes the discussion of the installing the leaky prediction to the motion picture coding method NUCLEI proposed before by the authors. NUCLEI is based on three strategies. The first, NUCLEI uses the interframe coding with the full band image signals. The second,

NUCLEI does the interframe coding after the occurring cell loss. The third, the image signals are divided to MSP(**Most Significant Part**) and LSP(**Least Significant Part**) by the measure of picture motion, not the frequency. On last proposal, the frame memory refresh method was by use of intraframe coding. But on the more low bit rate coding, the frame refresh method by the leaky prediction is needed. In this paper, the authors showed that the leaky prediction for NUCLEI as the frame memories refresh was effective with the discussion and the simulation. (author abst.)